Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (original) A semiconductor device comprising:

a collector layer of first conductive type formed on a semiconductor substrate;

a graft base layer of second conductive type formed in a surface region of the collector layer;

a first base leading-out region of second conductive type formed on the graft base layer;

a second base leading-out region of second conductive type formed on an upper surface and a side surface of the first base leading-out region;

a base layer of second conductive type formed on the collector layer;

an emitter layer of first conductive type formed in a surface region of the base layer; and

an emitter leading-out region formed on the emitter layer.

2. (original) A semiconductor device according to claim 1, wherein the base layer is also formed on the second base leading-out region, and at least part of an impurity concentration profile of the second base leading-out region is smaller than an impurity concentration of the first base leading-out region.

3. (original) A semiconductor device according to claim 1, wherein the first and second base leading-out regions are made of the same material.

4. (original) A semiconductor device according to claim 3, wherein the base layer is also formed on the second base leading-out region, and at least part of an impurity concentration profile of the second base leading-out region is smaller than an impurity concentration of the first base leading-out region.

5. (original) A semiconductor device according to claim 1, wherein the base layer is an epitaxial growth layer.

6. (original) A semiconductor device according to claim 5, wherein the base layer is made of SiGe.

7. (original) A method for manufacturing a semiconductor device, comprising:

forming a collector layer of first conductive type in a semiconductor substrate;

forming a first base leading-out region to which impurities of second conductive type are added on the collector layer to form a non-doped region on upper surface and a side surface of the first base leading-out region;

forming a base layer of second conductive type on the non-doped region and the collector layer;

thermally diffusing the impurities of second conductive type in the first base leading-out region into the non-doped region and the collector layer immediately below the first base leading-out region;

forming an emitter layer of first conductive type in a surface region of the base layer; and

forming an emitter leading-out region on the emitter layer.

8. (original) A method for manufacturing a semiconductor device according to claim 7, wherein the first and second base leading-out regions are made of the same material.

9. (original) A method for manufacturing a semiconductor device according to claim 7, wherein at least part of an impurity concentration profile of the second base leading-out region is smaller than an impurity concentration of the first base leading-out region.

10. (original) A method for manufacturing a semiconductor device according to claim 7, wherein the base layer is formed by epitaxial growth.

11. (original) A method for manufacturing a semiconductor device according to claim 10, wherein the epitaxial growth is non-selective epitaxial growth.

12. (original) A method for manufacturing a semiconductor device according to claim 10, wherein the base layer is made of SiGe.

13. (original) A method for manufacturing a semiconductor device, comprising:

forming a collector layer of first conductive type in a semiconductor substrate;

forming an element isolating region in the collector layer;

forming a dielectric pattern on part of the collector layer;

forming a first base leading-out region to which impurities of second conductive type are added on the collector layer where the dielectric pattern is not formed to form a first non-doped region on the first base leading-out region;

removing the dielectric pattern by wet-etching;

forming a second non-doped region on a side surface of the first base leading-out region and a side surface of the first non-doped region;

forming a base layer of second conductive type on the first and second non-doped regions and the collector layer;

thermally diffusing the impurities of second conductive type in the first base leading-out region into the first and second non-doped regions and the collector layer immediately below the first base leading-out region;

forming an emitter layer of first conductive type in a surface region of the base layer; and

forming an emitter leading-out region on the emitter layer.

14. (original) A method for manufacturing a semiconductor device according to claim 13, wherein the first and second base leading-out regions are made of the same material.

15. (original) A method for manufacturing a semiconductor device according to claim 13, wherein at least part of an impurity concentration profile of the second base leading-out region is smaller than an impurity concentration of the first base leading-out region.

16. (original) A method for manufacturing a semiconductor device according to claim 13, wherein the base layer is formed by epitaxial growth.

17. (original) A method for manufacturing a semiconductor device according to claim 16, wherein the epitaxial growth is non-selective epitaxial growth.

18. (original) A method for manufacturing a semiconductor device according to claim 16, wherein the base layer is made of SiGe.

19. (new) A semiconductor device according to claim 1, wherein the first and second base leading-out regions are made of polycrystalline silicon and the base layer is made SiGe, and wherein an impurity concentration of the base layer is lower than that of the first base leading-out region, and an impurity concentration profile of the second base leading-out region is substantially a middle impurity concentration profile between the impurity concentrations of the first base leading-out region which is the lower layer and the base layer which is the upper layer.